SPECIFICATION

[Title of the Invention]

MIM Capacitor Having High Capacitance and Integrated Circuit Chip Including the Same

[Brief Description of the Drawings]

The above and other aspects and advantages of the present invention will become more apparent by describing in detail preferred embodiments thereof with reference to the attached drawings in which:

FIGS. 1 and 2 are cross-sectional views of conventional MIM capacitors;

FIG. 3 is an equivalent circuit diagram of a MIM capacitor according to a first embodiment of the present invention;

FIG. 4 is a first layout diagram for realizing the MIM capacitor according to the first embodiment of the present invention;

FIGS. 5 through 7 are cross-sectional views of MIM capacitors formed according to the first layout shown in FIG. 4;

FIG. 8 is a second layout for realizing the MIM capacitor according to the first embodiment of the present invention;

FIGS. 9 through 11 are cross-sectional views of MIM capacitors formed according to the second layout diagram shown in FIG. 8;

FIGS. 12 and 13 are third and fourth layouts, respectively, for realizing the MIM capacitor according to the first embodiment of the present invention;

FIG. 14 is an equivalent circuit diagram of a MIM capacitor according to a second embodiment of the present invention;

FIGS. 15 and 16 are first and second layouts, respectively, for realizing the MIM capacitor according to the second embodiment of the present invention;

FIGS. 17 through 19 are cross-sectional views of MIM capacitors formed according to the first and second layouts shown in FIGS. 15 and 16, respectively;

FIG. 20 is an equivalent circuit diagram of a MIM capacitor according to a third embodiment of the present invention;

FIGS. 21 and 22 are first and second layouts for realizing the MIM capacitor according to the third embodiment of the present invention;

FIGS. 23 through 25 are cross-sectional views of MIM capacitors formed according to the first and second layouts shown in FIGS. 21 and 22, respectively;

FIGS. 26 through 29 are cross-sectional views illustrating a method for manufacturing a MIM capacitor shown in FIG. 5;

FIGS. 30 and 31 are cross-sectional views illustrating a method for manufacturing a MIM capacitor shown in FIG. 6; and

FIG. 32 is a cross-sectional view illustrating a method for manufacturing a MIM capacitor shown in FIG. 25.

[Detailed Description of the Invention]

[Object of the Invention]

[Technical Field of the Invention and Related Art prior to the Invention]

The present invention relates to a metal-insulator-metal (MIM) capacitor having high capacitance and an integrated circuit chip including the MIM capacitor.

Capacitors are divided into metal-oxide-silicon (MOS) capacitors, pn junction capacitors, polysilicon-insulator-polysilicon (PIP) capacitors, and MIM capacitors according to their junction structures. In all kinds of capacitors except for MIM capacitors, at least one electrode is formed of monocrystalline silicon or polycrystalline silicon. However, due to the physical characteristics of monocrystalline silicon or polycrystalline silicon, there has been a limit in reducing the resistance of a capacitor electrode. In addition, when a bias voltage is applied to a monocrystalline or polycrystalline silicon electrode, depletion may occur, the voltage may become unstable,

and finally, the capacitance of the silicon electrode can hardly be maintained at a certain level.

Therefore, a MIM capacitor, which is capable of reducing its dependence on frequency by reducing its resistance and has favorable rates of capacitance changing with voltage and temperature, i.e., a voltage coefficient and a temperature coefficient, has been applied to various kinds of analog products, mixed mode signal products, and system-on-a-chip (SOC) products. For example, such a MIM capacitor has been widely employed in an analog capacitor or filter for analog or mixed mode signal applications in wired or wireless communications, a decoupling capacitor of a main processing unit board, a radio-frequency (RF) capacitor of a high frequency circuit, and an embedded DRAM.

However, the manufacturing process of the conventional MIM capacitor has many problems due to the structural limits of the MIM capacitor. FIGS. 1 and 2 are cross-sectional views of two conventional MIM capacitors as taught by R. Liu et al., Proc. IITC, 111 (2000) and M. Armacost et al., Proc. IEDM, 157 (2000), respectively.

In FIGS. 1 and 2, reference numerals 10 and 12 indicate a MIM capacitor, and reference numerals 20, 30, 40, and 50 indicate a lower electrode, a dielectric layer, an upper electrode, and a capping layer, respectively. In addition, reference numerals C/P_20, C/P_40, C/H, D/D_20, D/D_40, and D/R indicate a lower electrode contact plug, an upper electrode contact plug, contact holes, a dual damascene wiring layer contacting a lower electrode, a dual damascene wiring layer contacting an upper electrode, and damascene regions, respectively. Other parts of the MIM capacitors 10 and 12, which are not accompanied by reference numerals, correspond to interlayer dielectric layers.

In the MIM capacitor 10 shown in FIG. 1, the upper electrode 40 and a wiring layer (not shown) through which a predetermined voltage is applied to the upper electrode 40 are electrically connected to each other by the upper electrode contact plug C/P_40. When forming the contact hole C/H, in which the upper electrode contact plug C/P_40 is supposed to be formed, it is difficult to precisely control an etching

process so as to make it be level with the top surface of the upper electrode 40. Therefore, the upper electrode 40 must be formed to have more than a predetermined thickness. However, as the thickness of the upper electrode 40 increases, the dielectric layer 30 under the upper electrode 40 is more likely to be exposed to an excessive etching process for patterning the upper electrode 40, and thus the lower electrode 20 may be exposed to the outside due to the dielectric layer 30 which is etched away. Therefore, the dielectric layer 30 must also be formed to have more than a predetermined thickness so that it can endure an excessive etching process, and this results in the decrease in the capacitance of the whole capacitor 10.

In the MIM capacitor 12 shown in FIG. 2, the dual damascene wiring layer D/D_40 through which a predetermined voltage is applied to the upper electrode 40 is electrically connected to the upper electrode 40. In order to obtain a sufficient margin for an etching process for forming the dual damascene region D/R, in which the dual damascene wiring layer D/D_40 is supposed to be formed, the thicknesses of the upper electrode 40 and the dielectric layer 30 must be increased, which accompanies the decrease in the capacitance of the whole capacitor 12.

In the MIM capacitor 10 shown in FIG. 1, the lower electrode contact plug C/P_20 and the upper electrode contact plug C/P_40 are formed in their respective contact holes C/H having a high aspect ratio but different depths. In the MIM capacitor 12 shown in FIG. 2, the dual damascene wiring layer D/D_40 and the dual damascene wiring layer D/D_20 are formed in their respective damascene regions D/R having a high aspect ratio but different depths. Accordingly, it is difficult to control processes for forming the contact holes C/H and the damascene regions D/R. In addition, there is a high probability of a bad electrical contact occurring due to byproducts, like polymer, generated during the formation of the contact holes C/H and the damascene regions D/R. In other words, the manufacturing process of a conventional MIM capacitor results in many disadvantages including limiting the capacitance of a capacitor. Therefore, development of a MIM capacitor having a new structure is required to realize a MIM capacitor having a high capacitance without including any limitations in the

manufacturing process.

[Technical Goal of the Invention]

To solve the above and other problems, it is an aspect of the present invention to provide a MIM capacitor having a high capacitance.

It is another aspect of the preset invention to provide an integrated circuit chip including the MIM capacitor.

[Structure and Operation of the Invention]

According to an aspect of the present invention, there is provided a metal-insulator-metal (MIM) capacitor including an upper electrode, a lower electrode, and a dielectric layer interposed between the upper and lower electrodes. A first voltage is applied to the upper electrode, and a second voltage is applied to the lower electrode. A wiring layer for applying the first voltage to the upper electrode is formed on a lower level than or on the same level as the lower electrode.

According to a first embodiment of the present invention, there is provided a MIM capacitor including: a first wiring layer and a second wiring layer which are formed on a substrate to be insulated from each other and to which a first voltage and a second voltage are respectively applied; a lower electrode whose level is higher than the first and second wiring layers and which is insulated from the first wiring layer and contacts the second wiring layer; and an upper electrode which overlaps the lower electrode with a dielectric layer formed therebetween and contacts the first wiring layer.

According to a second embodiment of the present invention, there is provided a MIM capacitor including: a first wiring layer to which a first voltage is applied; a lower electrode whose level is higher than the first wiring layer and which is insulated from the first wiring layer; and an upper electrode which overlaps the lower electrode with a dielectric layer interposed therebetween and contacts the first wiring layer.

According to a third embodiment of the present invention, there is provided a MIM capacitor including: a first wiring layer to which a first voltage is applied; a lower

electrode which is insulated from the first wiring layer and whose level is the same as the first wiring layer; and an upper electrode which overlaps the lower electrode with a dielectric layer interposed therebetween and contacts the first wiring layer.

According to another aspect of the present invention, there is provided an integrated circuit chip including one of the MIM capacitors according to the first, second, and third embodiments of the present invention.

The present invention will now be described more fully with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete and will fully convey the concept of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. It will also be understood that when a layer is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present. The same reference numerals in different drawings represent the same elements.

In a MIM capacitor according to a preferred embodiment of the present invention, a wiring layer through which a predetermined voltage is applied to an upper electrode is located in the same level as a lower electrode or in a lower level.

FIG. 3 is an equivalent circuit diagram of a MIM capacitor 100 according to a first embodiment of the present invention. The MIM capacitor 100 includes a lower electrode in an M_n level and an upper electrode in an M_{n+1} level. A first voltage V_1 is applied to the upper electrode in the M_{n+1} level via a wiring layer in an M_{n-1} level which is lower than the M_n level. A second voltage V_2 is applied to the lower electrode in the M_n level via a wiring layer in the M_{n-1} level. In this disclosure, M_{n-1} through M_{n+1} represent the levels of n-1-th through n+1-th wiring layers (here, n is an integer). Depending on the application, the levels of wiring layers may vary, and the positions of upper and lower electrodes and wiring layers may also vary.

A difference ($Vdiff = |V_2 - V_1|$) between the first and second voltages V_1 and V_2 satisfies the following equation.

$$Q = CVdiff \quad \cdots(1)$$

In Equation (1), Q and C represent the quantity of electric charge and capacitance, respectively.

As shown in Equation (1), Vdiff may vary depending on how much electric charge a MIM capacitor is required to have.

In conventional devices, Vdiff corresponds to a difference between a power supply voltage Vdd and a ground voltage.

The MIM capacitor 100 shown in FIG. 3 may be embodied using a first layout shown in FIG. 4. In FIG. 4, reference numerals 112, 114, 120, 140, and C/H1 represent a pattern for a first wiring layer to which the first voltage V_1 is applied, a pattern for a second wiring layer to which the second voltage V_2 is applied, and a pattern for a lower electrode, a pattern for an upper electrode, a pattern for a contact hole which exposes the first wiring layer.

MIM capacitors formed using the first layout diagram shown in FIG. 4 may have different cross-sectional shapes, as shown in FIGS. 5 through 7, which are cross-sectional views of such MIM capacitors, taken along line A – A' of FIG. 4.

Referring to FIG. 5, a MIM capacitor has a structure in which an upper electrode 140 is arranged to overlap a lower electrode 120, and a dielectric layer 130 is interpolated between the upper and lower electrodes 140 and 120. The upper electrode 140 contacts the first wiring layer 112, to which the first voltage V_1 is applied, through the contact hole C/H1 which is formed in the dielectric layer 130 to expose the first wiring layer 112. The contact hole C/H1 is formed before the upper electrode 140 is formed so that the contact hole C/H1 can be connected to the bottom of the contact hole C/H1. Accordingly, the contact hole C/H1 is completely different from the contact holes C/H and the damascene regions D/R in the conventional MIM capacitors 10 and

12 shown in FIGS. 1 and 2 because the contact holes C/H and the damascene regions D/R are formed to expose the top surface of the upper electrode 40. In addition, since the thickness of the dielectric layer 130, in which the contact hole C/H1 is formed, is very small, the aspect ratio of the contact hole C/H1 is also very small. Accordingly, the problems accompanied by the contact holes C/H or the damascene regions D/R, which are formed having a high aspect ratio, are much less likely to occur in the present embodiment.

The upper electrode 140 is formed of a conductive layer in the M_{n+1} level, and the first wiring layer 112 is formed of a conductive layer in the M_{n-1} level. The lower electrode 120 is formed of a conductive layer in the M_n level to directly contact the second wiring layer, to which the second voltage V_2 is applied. The second wiring layer 114 is formed of a conductive layer in the same level as the first wiring layer 112.

It is preferable to form the first and second wiring layers 112 and 114 to have a planarized top surface to minimize a step difference. Therefore, as shown in FIG. 5, the first and second wiring layers 112 and 114 are formed of a damascene wiring layer embedded in an interlayer dielectric layer 105. The damascene wiring layer is formed by depositing a conductive layer in trenches T_1 and T_2 formed in the interlayer dielectric layer 105 and performing chemical mechanical polishing (CMP) so as to planarize the conductive layer. The process of manufacturing the damascene wiring layer will be described more fully later. The damascene wiring layer is comprised of a barrier metal layer 110 formed at the inner sidewalls and bottom surface of each of the trenches T_1 and T_2 and a planarized conductive layer 111 filling the trenches T_1 and T_2.

The upper electrode 140 is covered with an upper interlayer dielectric layer so that it can be insulated from an upper structure (not shown). The upper interlayer dielectric layer is preferably comprised of a capping layer 150 for protecting the upper electrode 140 and an interlayer dielectric layer 155.

Connections between the first and second wiring layers 112 and 114 and other wiring layers and processes of manufacturing wiring layers in a level higher than the M_{n+1} level may vary depending on the application.

The sizes of the upper and lower electrodes 140 and 120 may vary depending on the application, preferably, to maximize the effective area of a capacitor electrode, i.e., the surface area of the upper and lower electrodes 140 and 120 facing each other.

In FIG. 6, unlike in the structure shown in FIG. 5 where the first and second wiring layers 112 and 114 are formed by performing CMP on conductive layers, the first and second wiring layers 112 and 114 are formed to be embedded in the interlayer dielectric layer 105 by performing CMP on the interlayer dielectric layer 105 so that the step difference can be minimized. In particular, a conductive layer is formed on a lower interlayer dielectric layer 102 and is patterned using a conventional photolithography process, thus forming patterns for the first and second wiring layers 112 and 114. Next, the interlayer dielectric layer 105 is deposited on the lower interlayer dielectric layer 102, and a CMP process is performed on the interlayer dielectric layer 105 so that it can be level with the top surfaces of the patterns for the first and second wiring layers 112 and 114. As a result of the CMP process, the top surfaces of the patterns for the first and second wiring layers 112 and 114 are level. Other elements of the MIM capacitor shown in FIG. 6 and their structures are the same as the corresponding elements of the MIM capacitor shown in FIG. 5 and their structures.

Referring to FIG. 7, first and second wiring layers 112 and 114 are very thin and thus do not need to be planarized. Alternatively, a MIM capacitor is realized without performing CMP if the surfaces of the first and second wiring layers 112 and 114 are required to be smooth. In particular, the first and second wiring layers 112 and 114 are wiring patterns formed on a lower interlayer dielectric layer 102 by patterning. A lower electrode 120 is patterned so as to be isolated from the first wiring layer 112 but to directly contact the second wiring layer 114. The isolation of the first wiring layer 112 from the lower electrode 120 is realized by a dielectric layer 130. Other elements of the MIM capacitor shown in FIG. 7 and their structures are the same as the corresponding elements of the MIM capacitor shown in FIG. 5 and their structures.

FIG. 8 is a second layout for realizing the MIM capacitor according to the first embodiment of the present invention. The second layout is different from the first layout only in the fact that a pattern for a contact hole C/H2, through which the top surface of a second wiring layer will be exposed, is further included.

FIGS. 9 through 11 are cross-sectional views of MIM capacitors using the second layout shown in FIG. 8, taken along line B – B' of FIG. 8.

Referring to FIG. 9, an upper interlayer dielectric layer 115 is formed on a lower interlayer dielectric layer 105, in which first and second wiring layers 112 and 114 are embedded, and a lower electrode 120 is formed on the interlayer dielectric layer 115. The lower electrode 120 is the same as the corresponding element of FIG. 5 except that it is formed to directly contact the second wiring layer 114 through the contact hole C/H2 formed in the upper interlayer dielectric layer 115, and an upper electrode 140 is formed to directly contact the first wiring layer 112 through a contact hole C/H1 formed in a dielectric layer 130 and the upper interlayer dielectric layer 115. In the MIM capacitor shown in FIG. 9, the contact hole C/H1 has a low aspect ratio since the contact hole C/H1 is formed in the dielectric layer 130 and the upper interlayer dielectric layer 115.

Referring to FIG. 10, CMP is performed on an interlayer dielectric layer 105 so as to make the top surfaces of first and second wiring layers 112 and 114 be level with each other. As a result of the CMP, the first and second wiring layers 112 and 114 are embedded in the interlayer dielectric layer 105, which is the difference between the MIM capacitor shown in FIG. 10 and the MIM capacitor shown in FIG. 9.

A MIM capacitor shown in FIG. 11 is the same as the one shown in FIG. 9 except that an interlayer dielectric layer 115 is formed after patterning the first and second wiring layers 112 and 114, without performing CMP.

FIGS. 12 and 13 are third and fourth layouts for realizing the MIM capacitor according to the first embodiment of the present invention. The third and fourth layouts are different from the first and second layouts in the fact that patterns for contact holes C/H1' and C/H2' are comprised of a plurality of divided patterns.

FIG. 14 is an equivalent circuit diagram of a MIM capacitor 200 according to a second embodiment of the present invention. The MIM capacitor 200 includes a lower electrode formed in the M_n level and an upper electrode formed in the M_{n+1} level. A first voltage V_1 is applied to the upper electrode via a wiring layer formed in the M_{n-1} level, which is lower than the level of the lower electrode. A second voltage V_2 is applied to the lower electrode via a wiring layer formed in an M_x level (here, $x > n+1$).

The MIM capacitor 200 according to the second embodiment of the present invention, which is shown in FIG. 14, may be embodied using the first or second layout diagram shown in FIG. 15 or 16, respectively. In FIG. 15, reference numerals 212, 220, and 240 represent a first wiring layer pattern, to which the first voltage V_1 is applied, a lower electrode pattern, and an upper electrode pattern, respectively. Reference numerals C/H1 and C/H3 represent a contact hole pattern for exposing the first wiring layer 212 and a contact hole pattern for exposing the lower electrode 220, respectively. FIG. 16 is a layout for realizing a MIM capacitor so that the effective area of the MIM capacitor can be maximized even more. The layout shown in FIG. 16 is the same as the one shown in FIG. 15 except that a lower electrode pattern 220 has a protrusion along one edge and the contact hole pattern C/H3 is arranged in the protrusion. As shown in FIGS. 12 and 13, the contact hole patterns C/H2 and C/H3 may be replaced by a plurality of divided patterns.

The cross-sections of MIM capacitors realized using the first or second layout shown in FIG. 15 or 16, respectively, have different structures, as shown in FIGS. 17 through 19.

Referring to FIG. 17, a MIM capacitor has a structure where an upper electrode 240 is arranged to overlap a lower electrode 220, and a dielectric layer 230 is interpolated between the upper and lower electrodes 240 and 220. The upper electrode 240 contacts a first wiring layer 212, to which the first voltage V_1 is applied, via a contact hole C/H1, through which the top surface of the first wiring layer 212 is exposed. The upper electrode 240 is formed of a conductive layer in the M_{n+1} level, the first wiring layer 212 is formed of a conductive layer in the M_{n-1} level, and the lower

electrode 220 is formed of a conductive layer in the M_n level. The lower electrode 220 contacts a second wiring layer (not shown) in the M_x level (here, x>n+1), to which the second voltage V_2 is applied, via a contact plug C/P_220 which fills a contact hole C/H3. The contact hole C/H3 is formed in upper interlayer dielectric layers 255 and 250 and a dielectric layer 230 so as expose the top surface of the lower electrode 220. Even though the lower electrode 220 is connected to the second wiring layer via the contact plug C/P_220, it is possible to form a MIM capacitor according to the present invention with the thickness of a dielectric layer minimized.

FIG. 18 shows the structure of a MIM capacitor, in which a first wiring layer 212 is embedded in an interlayer dielectric layer 205 planarized by performing CMP, and FIG. 19 shows the structure of another MIM capacitor which is the same as that of the MIM capacitor shown in FIG. 17 except that a first wiring layer 212 is isolated from a lower electrode 220 by forming another interlayer dielectric layer 215 after forming the first wiring layer 212 on a lower interlayer dielectric layer 2102 without performing CMP.

FIG. 20 is an equivalent circuit diagram of a MIM capacitor 300 according to a third embodiment of the present invention. The MIM capacitor 300 includes a lower electrode formed in the M_n level and an upper electrode formed in the M_{n+1} level. The first voltage V_1 is applied to the upper electrode via a wiring layer formed in the same level (M_n) as the lower electrode. The second voltage V_2 is applied to the lower electrode of the Mn level via a wiring layer formed in an M_x level (here, x>n+1).

The MIM capacitor 300 according to the third embodiment may be embodied using the first or second layout shown in FIG. 21 or 22, respectively. In FIG. 21, reference numerals 320, 322, and 340 represent a lower electrode pattern, a first wiring layer pattern, to which the first voltage V_1 is applied, and an upper electrode pattern, respectively. Reference numerals C/H1 and C/H2, respectively, represent a contact hole pattern, through which a first wiring layer is exposed, and a contact hole, through which a lower electrode is exposed. FIG. 22 is a layout diagram for realizing a MIM capacitor so as to maximize the effective area of the MIM capacitor even more. The layout shown in FIG. 22 is the same as the one shown in FIG. 21 except that the lower

electrode pattern 220 has a protrusion along one edge and the contact hole pattern C/H3 is arranged in the protrusion. As shown in FIGS. 12 and 13, the contact hole patterns C/H2 and C/H3 may be replaced by a plurality of divided patterns.

The cross-sections of MIM capacitors embodied using the first or second layout shown in FIG. 21 or 22 may have different structures, as shown in FIGS. 23 through 25, which are cross-sectional diagrams of such MIM capacitors, taken along lines D – D' of FIGS. 21 and 22.

Referring to FIG. 23, an upper electrode 340 is arranged to overlap a lower electrode 320, and a dielectric layer 330 is interpolated between the upper and lower electrodes 340 and 320. The upper electrode 340 contacts a first wiring layer 322, to which the first voltage V_1 is applied, through a contact hole C/H1 which is formed in the dielectric layer 330 to expose the first wiring layer 322. The upper electrode 340 is formed of a conductive layer in the M_{n+1} level, the first wiring layer 322 is formed of a conductive layer in the M_n level, and the lower electrode 320 is formed of a conductive layer of the M_n level. A contact plug C/P_320 is formed to fill the contact hole C/H3 which is formed in interlayer dielectric layers 355 and 350 and the dielectric layer 330 to expose the top surface of the lower electrode 320. The lower electrode 320 is connected to a second wiring layer (not shown) in the M_x level (here, x>n+1), through which the second voltage V_2 is applied to the lower electrode 320, via the contact plug C/P_320 which is formed to bury the contact hole C/H3.

In terms of minimizing a step difference, it is preferable that the top surfaces of the lower electrode 320 and the first wiring layer 322 are level with each other. In FIG. 23, the lower electrode 320 and the first wiring layer 322 are damascene wiring layers which are formed by depositing a conductive layer in trenches T_b and T_2, which are formed in a dielectric layer 305, and planarizing the conductive layer using CMP. The damascene wiring layers are comprised of a barrier metal layer 310 formed at the inner walls and bottom of each of the trenches T_b and T_2 and a planarized conductive layer 311 formed filling the trenches T_b and T_2. Connections between the first wiring layer

322 and other wiring layers and processes for manufacturing wiring layers in a level higher than the M_{n+1} level may vary depending on the application.

A MIM capacitor shown in FIG. 24 is the same as the MIM capacitor shown in FIG. 23 except that a lower electrode 320 and a first wiring layer 322 are located on a lower interlayer dielectric layer 302 and are embedded in an interlayer dielectric layer 305 which has been planarized by performing CMP.

Referring to FIG. 25, a lower electrode 320 and a first wiring layer 322 are formed on a lower interlayer dielectric layer 302 to be very thin. Thus, it is possible to realize a MIM capacitor without performing a CMP process if the lower electrode 320 and the first wiring layer 322 can be electrically disconnected using only a dielectric layer 330.

Hereinafter, a method for manufacturing the MIM capacitor shown in FIG. 5 using the first layout shown in FIG. 4, which is for realizing a MIM capacitor according to the first embodiment of the present invention will be described with reference to FIGS. 26 through 29.

Referring to FIG. 26, trenches T_1 and T_2 are formed in an interlayer dielectric layer 105 on a substrate (not shown) including a wiring layer, in an M_{n-2} level. A barrier layer 110 is formed at the inner walls and bottom of each of the first and second trenches T_1 and T_2. The barrier layer 110 may be formed of a transition metal layer, a transition metal alloy layer, or a transition metal compound layer, or any combination thereof. For example, the barrier layer 110 may be formed of a Ta layer, a TaN layer, a TaSiN layer, a TiN layer, a TiSiN layer, a WN layer, or a WSiN layer. The barrier layer 110 is introduced to prevent metal atoms of the metal layer filling the first and second trenches T_1 and T_2 from diffusing into the interlayer dielectric layer 105. Next, a conductive layer 111, for example, a metal layer, is formed on the barrier layer 110 so as to completely fill the first and second trenches T_1 and T_2.

The conductive layer 111 may be formed of any low-resistance material that is appropriate for damascene processes. For example, the conductive layer 111 may be formed of a copper (Cu) layer. In particular, a copper seed layer is formed on the

barrier layer 110 which is formed at the inner walls and bottom of each of the trenches T_1 and T_2. Next, the conductive layer 111 comprised of a copper layer is formed on the copper seed layer to completely fill the trenches T_1 and T_2 using electroplating.

Thereafter, as shown in FIG. 27, the conductive layer 111 and the barrier layer 110 are planarized using CMP until the top surface of the interlayer dielectric layer 105 is exposed. As a result of the planarization, wiring layers of an M_{n-1} level, i.e., first and second wiring layers 112 and 114, are formed without a step difference therebetween.

Next, a conductive level of a M_n level is deposited on the entire surface of the substrate and is patterned using conventional photolithography so that a lower electrode 120 is formed to directly contact the second wiring layer. The lower electrode 120 may be formed of one selected from among a metal layer, a metal compound layer, and a combination thereof. For example, the lower electrode 120 may be formed of an Al layer, a Ta layer, a TaN layer, a TaSiN layer, a TiN layer, a TiSiN layer, a WN layer, a WSiN layer, or any combination thereof. Alternatively, the lower electrode 120 may be formed of a double layer of a Ta layer and a Cu layer, a double layer of a TaN layer and a Cu layer, a triple layer of a Ta layer, a TaN layer, and a Cu layer, or a triple layer of a TiN layer, a AlCu layer, and a TiN layer.

Next, as shown in FIG. 28, a dielectric layer 130 is formed on the entire surface of the substrate, on which the lower electrode 120 is formed, and is patterned, thus forming a contact hole C/H1 through which the first wiring layer 112 is exposed. The dielectric layer 130 may be formed of any material as long as the dielectric constant of the material is high enough to enhance the capacitance of a whole MIM capacitor. For example, the dielectric layer 130 may be formed of a SiO_2 layer, a Si_xN_y layer, a Si_xC_y layer, a $Si_xO_yN_z$ layer, a $Si_xO_yC_z$ layer, an Al_xO_y layer, a Hf_xO_y layer, or a Ta_xO_y layer. If the lower electrode 120 is formed of a copper-based material, the dielectric layer 130 is preferably formed of a Si_xN_y layer, a Si_xC_y layer, a double layer of a Si_xN_y layer and an oxide layer, or a double layer of a Si_xC_y layer and an oxide layer. For example, the dielectric layer 130 may be formed of a double layer of a Si_xN_y layer and a $Si_xO_yC_z$ layer, a double layer of a Si_xN_y layer and a TEOS layer, a double layer of Si_xN_y layer and a

PEOX layer, a double layer of Si_xC_y layer and a $Si_xO_yC_z$ layer, a double layer of a Si_xC_y layer and a TEOS layer, or a double layer of a Si_xC_y layer and a PEOX layer. It is possible to enhance the leakage current characteristics of a capacitor by forming the dielectric layer 130 of a double layer of a Si_xN_y layer and an oxide layer or a double layer of a Si_xC_y layer and an oxide layer.

The capacitance of a capacitor can be calculated following Equation (2).

$$C = \varepsilon \times \frac{A}{d} \quad \cdots(2)$$

In Equation (2), C, ε, A, and d represent capacitance, a dielectric constant, the effective area of capacitor electrodes, and a distance between electrodes, respectively.

As shown in Equation (2), it is possible to increase capacitance by increasing the effective area (A) of capacitor electrodes, decreasing the distance (d) between electrodes, or forming the dielectric layer 130 of a material having a high dielectric constant ε.

In other words, the thickness of the dielectric layer 130 may vary depending on the desired capacitance. For example, if the dielectric layer 130 is formed of a SiO_2 layer having a dielectric constant of 3.9, the electric layer 130 is preferably formed to have a thickness of about 345 Å. If the dielectric layer 130 is formed of a Si_xN_y layer having a dielectric constant of 7.5, the dielectric layer 130 is preferably formed to have a thickness of about 664 Å. In both of the two cases, the capacitance per unit area of the capacitor is $1.0fF/\mu m^2$.

Thereafter, a conductive layer of a M_{n+1} level is deposited on the entire surface of the substrate and is patterned using conventional photolithography, thus forming an upper electrode 140 to contact the first wiring layer 112 via the contact hole C/H1. Here, the upper electrode 140 may be formed of the same conductive layer as the lower electrode 120.

Next, as shown in FIG. 29, a capping layer 150 and an interlayer dielectric layer 155 are sequentially formed to protect the upper electrode 140. The capping layer 150 and the interlayer dielectric layer 155 may be formed of a TEOS layer, a PEOX layer, a $Si_xO_yC_z$ layer, a $Si_xO_yF_z$ layer, or a Si_xN_y layer. Connections between the first and second wiring layers 112 and 114 and other wiring layers and processes of manufacturing wiring layers in a level higher than the M_{n+1} level may vary depending on the application.

FIGS. 30 and 31 are cross-sectional views illustrating a method of manufacturing the MIM capacitor shown in FIG. 6 using the first layout shown in FIG. 4, which is for realizing a MIM capacitor according to the first embodiment of the present invention.

As shown in FIG. 30, a conductive layer of a M_{n-1} level is formed on a lower interlayer dielectric layer 102 and is patterned using conventional photolithography, thus forming first and second wiring layers 112 and 114. An interlayer dielectric layer 105 is formed having a predetermined thickness so that the first and second wiring layers 112 and 114 can be isolated from each other.

As shown in FIG. 31, a CMP process is performed on the interlayer dielectric layer 105 so that it can be level with the top surfaces of the first and second wiring layers 112 and 114. As a result of the CMP process, the first and second wiring layers 112 and 114 are electrically isolated and planarized. Subsequent processes are the same as the corresponding processes described above with reference to FIGS. 27 through 29.

MIM capacitors having the cross-sections shown in FIGS. 7, 9 through 11, 17 through 19, 23, and 24 may be embodied in various ways using the above-described manufacturing processes and other arbitrary methods which are well known to one skilled in the art.

Hereinafter, a method for manufacturing the MIM capacitor according to the third embodiment of the present invention, which is shown in FIG. 25, will be described with reference to FIG. 32.

A conductive layer of a M_n level is formed on a lower interlayer dielectric layer 302 and is patterned using conventional photolithography, thus forming a lower electrode 320 and a first wiring layer 322. Next, a dielectric layer 330 is deposited and is patterned, thus forming a contact hole C/H1, through which the first wiring layer 322 is exposed. Subsequent processes may be performed using arbitrary methods which are well known to the one in the art, thus forming a MIM capacitor having the cross-section shown in FIG. 25.

While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.

[Effect of the Invention]

According to the present invention, a wiring layer through which a predetermined voltage is applied to an upper electrode is formed in a level lower than a lower electrode or in the same level as the lower electrode, and thus the wiring layer is formed before forming the upper electrode instead of forming a contact hole on the upper electrode to make the wiring layer contact the upper layer. Accordingly, the upper electrode and a dielectric layer do not need to be formed as thick as they used to be in the conventional techniques. In other words, it is possible to minimize the thickness of the dielectric layer as much as possible while maintaining the reliability of the dielectric layer to some extent. Therefore, it is possible to realize a MIM capacitor having a high capacitance. In addition, according to the present invention, a contact hole, through which the upper electrode and a wiring layer contact each other, is formed having a low aspect ratio, and thus it is possible to reduce the probability of the problems with a conventional contact hole or a damascene region having a high aspect ratio from occurring.